

# 1995 Index

## IEEE Transactions on Semiconductor Manufacturing

### Vol. 8

This index covers all technical items - papers, correspondence, reviews, etc. - that appeared in this periodical during 1995, and items from previous years that were commented upon or corrected in 1995.

The Author Index contains the primary entry for each item, listed under the first author's name, and cross-references from all coauthors. The Subject Index contains several entries for each item under appropriate subject headings, and subject cross-references.

It is always necessary to refer to the primary entry in the Author Index for the exact title, coauthors, and comments/corrections.

#### AUTHOR INDEX

##### A

Adams, R., *see* Roedel, R.J., *T-SEM Feb 95 79-83*  
Akiya, H., *see* Itsumi, M., *T-SEM Aug 95 365-370*

##### B

Baker, M.D., C.D. Himmel, and G.S. May. Time series modeling of reactive ion etching using neural networks; *T-SEM Feb 95 62-71*  
Baliga, B.J., *see* Venkatraman, P., *T-SEM Nov 95 451-453*  
Bartelink, D.J., *see* Crid Yu, *T-SEM May 95 150-159*  
Bauer, H., P. Pichler, and H. Ryssel. Modeling dynamic clustering of arsenic including non-negligible concentrations of arsenic-point defect pairs; *T-SEM Nov 95 414-418*  
Bechtold, P.F., *see* Kizilyalli, I.C., *T-SEM Nov 95 440-448*  
Belikov, S., H. Martynov, M. Kaplinsky, and C. Manikopoulos. Using wavelength-dependent emissivity of semiconductor wafer to model heat transfer in rapid thermal processing station; *T-SEM Aug 95 360-362*  
Ben-tzur, M., *see* Riley, P.E., *T-SEM Aug 95 309-313*  
Berglund, C.N., *see* Jun Ye, *T-SEM Aug 95 319-325*  
Bielle-Daspert, D., *see* Campo, E., *T-SEM Aug 95 298-303*  
Bielle-Daspert, D., *see* Henda, R., *T-SEM Aug 95 362-365*  
Bohmayr, W., A. Burenkov, J. Lorenz, H. Ryssel, and S. Selberherr. Trajectory split method for Monte Carlo simulation of ion implantation; *T-SEM Nov 95 402-407*  
Bohn, R.E. The impact of process noise on VLSI process improvement; *T-SEM Aug 95 228-238*  
Boning, D.S., *see* Crid Yu, *T-SEM May 95 150-159*  
Boskin, E.D., *see* Lee, S.F., *T-SEM Feb 95 17-25*  
Bozada, C.A., *see* DeSalvo, G.C., *T-SEM Aug 95 314-318*  
Bruls, E. Quality and reliability impact of defect data analysis; *T-SEM May 95 121-129*  
Burenkov, A., *see* Bohmayr, W., *T-SEM Nov 95 402-407*  
Burkett, S.L., E.M. Charlson, E.J. Charlson, H.K. Yasuda, and Duck-Joo Yang. The effect of cleaning procedures on surface charging of various substrates; *T-SEM Feb 95 10-16*  
Busch-Vishniac, I.J., *see* Chen, S.-J.S., *T-SEM Feb 95 72-78*  
Busch-Vishniac, I.J., *see* Leifer, J., *T-SEM Aug 95 352-359*

##### C

Camilletti, L., *see* Nanz, G., *T-SEM Nov 95 382-389*  
Campo, E., E. Scheid, D. Bielle-Daspert, and J.-P. Guillemet. Influence of rapid thermal and low temperature processing on the electrical properties of polysilicon thin film transistors; *T-SEM Aug 95 298-303*  
Card, J.P., *see* Collica, R.S., *T-SEM Aug 95 326-332*  
Cardarelli, E., and P.M. Pelagagge. Simulation tool for design and management optimization of automated interbay material handling and storage systems for large wafer fab; *T-SEM Feb 95 44-49*  
Chang Keh-Jeng, *see* Crid Yu, *T-SEM May 95 150-159*  
Chao Chieh-Yuan, *see* Chieh-Yuan Chao, *T-SEM Aug 95 239-251*  
Charlson, E.J., *see* Burkett, S.L., *T-SEM Feb 95 10-16*  
Charlson, E.M., *see* Burkett, S.L., *T-SEM Feb 95 10-16*  
Cheek, G., *see* De Gyvez, J.P., *T-SEM May 95 93-94*  
Chen, S.-J.S., and I.J. Busch-Vishniac. A magnetically levitated, automated, contact analytical probe tool; *T-SEM Feb 95 72-78*  
Cheng Liu Hao, *see* Lee, S.F., *T-SEM Feb 95 17-25*

Chenming Hu, *see* Minami, E.R., *T-SEM Aug 95 370-374*  
Chieh-Yuan Chao, and L.S. Milor. Performance modeling using additive regression splines; *T-SEM Aug 95 239-251*  
Chiluvuri, V.K.R., and I. Koren. Layout-synthesis techniques for yield enhancement; *T-SEM May 95 178-187*  
Chung, J.E., *see* Crid Yu, *T-SEM May 95 150-159*  
Cochran, W.T., *see* Kizilyalli, I.C., *T-SEM Nov 95 440-448*  
Collica, R.S., J.P. Card, and W. Martin. SRAM bitmap shape recognition and sorting using neural networks; *T-SEM Aug 95 326-332*  
Crid Yu, Tinaung Maung, C.J. Spanos, D.S. Boning, J.E. Chung, Hua-Yu Liu, Keh-Jeng Chang, and D.J. Bartelink. Use of short-loop electrical measurements for yield improvement; *T-SEM May 95 150-159*  
Cullen, C.W., and J.C. Sturm. Temperature measurement of metal-coated silicon wafers by double-pass infrared transmission; *T-SEM Aug 95 346-351*  
Cunningham, S.P., C.J. Spanos, and K. Voros. Semiconductor yield improvement: results and best practices; *T-SEM May 95 103-109*

##### D

Davito, D., *see* Roedel, R.J., *T-SEM Feb 95 79-83*  
De Gyvez, J.P., *see* Kumar, R.C.K., *T-SEM Feb 95 84-87*  
De Gyvez, J.P., and G. Cheek. Editorial [intro. to special issue on advanced yield modeling]; *T-SEM May 95 93-94*  
DeSalvo, G.C., T.K. Quach, C.A. Bozada, R.W. Dettmer, K. Nakano, J.K. Gillespie, G.D. Via, J.L. Ebel, and C.K. Havasy. Simplified ohmic and Schottky contact formation for field effect transistors using the single layer integrated metal field effect transistor (SLIMFET) process; *T-SEM Aug 95 314-318*  
Dettmer, R.W., *see* DeSalvo, G.C., *T-SEM Aug 95 314-318*  
Deweerd, B., *see* Wang, Q., *T-SEM Nov 95 449-451*  
Dilhac, J.-M., N. Nohier, C. Ganibal, and C. Zanchi. Thermal modeling of a wafer in a rapid thermal processor; *T-SEM Nov 95 432-439*  
Dimitrijević, S., *see* Sitte, R., *T-SEM Aug 95 374-377*  
Duck-Joo Yang, *see* Burkett, S.L., *T-SEM Feb 95 10-16*  
Duncan, A., *see* Kizilyalli, I.C., *T-SEM Nov 95 440-448*  
Dutta, M., *see* Weber, C., *T-SEM May 95 110-120*  
Dutton, R.W., *see* Park, H., *T-SEM Nov 95 390-401*

##### E

Ebel, J.L., *see* DeSalvo, G.C., *T-SEM Aug 95 314-318*  
Elta, M.E., *see* Rashap, B.A., *T-SEM Aug 95 286-297*  
Etemad, H., *see* Rashap, B.A., *T-SEM Aug 95 286-297*

##### F

Fenstermaker, L.R., *see* Kizilyalli, I.C., *T-SEM Nov 95 440-448*  
Fordham, M.J., *see* Sorrell, F.Y., *T-SEM Aug 95 280-285*  
Fournier, J.P., *see* Rashap, B.A., *T-SEM Aug 95 286-297*  
Freudenberg, J.S., *see* Rashap, B.A., *T-SEM Aug 95 286-297*  
Freyman, R., *see* Kizilyalli, I.C., *T-SEM Nov 95 440-448*

##### G

Gaitonde, D.D., and D.M.H. Walker. Hierarchical mapping of spot defects to catastrophic faults-design and applications; *T-SEM May 95 167-177*  
Ganibal, C., *see* Dilhac, J.-M., *T-SEM Nov 95 432-439*  
Giles, M.D., *see* Rashap, B.A., *T-SEM Aug 95 286-297*  
Gillespie, J.K., *see* DeSalvo, G.C., *T-SEM Aug 95 314-318*  
Griep, S., *see* Khare, J.B., *T-SEM May 95 195-206*  
Grizzle, J.W., *see* Rashap, B.A., *T-SEM Aug 95 286-297*  
Guillemet, J.-P., *see* Campo, E., *T-SEM Aug 95 298-303*  
Gyuresik, R.S., *see* Perkins, R.H., *T-SEM Aug 95 272-279*

##### H

Hao Cheng Liu, *see* Lee, S.F., *T-SEM Feb 95 17-25*  
Harrison, H.B., *see* Sitte, R., *T-SEM Aug 95 374-377*  
Havasy, C.K., *see* DeSalvo, G.C., *T-SEM Aug 95 314-318*



- Henda, R., E. Scheid, and D. Bielle-Daspert. Investigation of the thermal behavior of a RTP furnace; *T-SEM Aug 95* 362-365  
 Himmel, C.D., *see* Baker, M.D., *T-SEM Feb 95* 62-71  
 Hong Xie, *see* Jian Tan, *T-SEM Feb 95* 50-61  
 Hong Xie, R.L. Mahajan, and Yung-Cheng Lee. Fuzzy logic models for thermally based microelectronic manufacturing processes; *T-SEM Aug 95* 219-227  
 Hu, A., *see* Sachs, E., *T-SEM Feb 95* 26-43  
 Hua Xue, *see* Huijbregts, E.P., *T-SEM May 95* 188-194  
 Hua-Yu Liu, *see* Crid Yu, *T-SEM May 95* 150-159  
 Hu Chenming, *see* Minami, E.R., *T-SEM Aug 95* 370-374  
 Huijbregts, E.P., Hua Xue, and J.A.G. Jess. Routing for reliable manufacturing; *T-SEM May 95* 188-194  
 Hunt, W.D., *see* Kenney, J.S., *T-SEM May 95* 207-213  
 Hwang, H., *see* Park, H., *T-SEM Nov 95* 390-401

## I

- Ingolfsson, A., *see* Sachs, E., *T-SEM Feb 95* 26-43  
 Itsumi, M., H. Akiya, S. Nakayama, and H. Yoshino. Spectrum analysis and vector representation of SRAM bit failures; *T-SEM Aug 95* 365-370

## J

- Jess, J.A.G., *see* Huijbregts, E.P., *T-SEM May 95* 188-194  
 Jian Tan, Hong Xie, and Yung-Cheng Lee. Efficient establishment of a fuzzy logic model for process modeling and control; *T-SEM Feb 95* 50-61  
 Jun Ye, C.N. Berglund, J. Robinson, and R.F.W. Pease. A review of mask errors on a variety of pattern generators; *T-SEM Aug 95* 319-325

## K

- Kabamba, P.T., *see* Rashap, B.A., *T-SEM Aug 95* 286-297  
 Kaempf, U. The binomial test: a simple tool to identify process problems; *T-SEM May 95* 160-166  
 Kaplinsky, M., *see* Belikov, S., *T-SEM Aug 95* 360-362  
 Kavari, R., *see* Riley, P.E., *T-SEM Aug 95* 309-313  
 Kearney, J.W., *see* Kizilyalli, I.C., *T-SEM Nov 95* 440-448  
 Keh-Jeng Chang, *see* Crid Yu, *T-SEM May 95* 150-159  
 Kenney, J.S., G.S. May, and W.D. Hunt. Yield modeling of acoustic charge transport transversal filters; *T-SEM May 95* 207-213  
 Khare, J.B., W. Maly, S. Griep, and D. Schmitt-Landsiedel. Yield-oriented computer-aided defect diagnosis; *T-SEM May 95* 195-206  
 Khargonekar, P.P., *see* Rashap, B.A., *T-SEM Aug 95* 286-297  
 Kizilyalli, I.C., M.J. Thoma, S.A. Lytle, E.P. Martin, Jr., R. Singh, S.C. Vitkavage, P.F. Bechtold, J.W. Kearney, M.M. Rambaud, M.S. Twiford, W.T. Cochran, L.R. Fenstermaker, R. Freyman, W. Sun, and A. Duncan. High performance 3.3- and 5-V 0.5- $\mu$ m CMOS technology for ASIC's; *T-SEM Nov 95* 440-448  
 Klein, K.M., *see* Morris, S.J., *T-SEM Nov 95* 408-413  
 Ko, P.K., *see* Minami, E.R., *T-SEM Aug 95* 370-374  
 Koren, I., *see* Wagner, I.A., *T-SEM May 95* 130-138  
 Koren, I., *see* Chiluvuri, V.K.R., *T-SEM May 95* 178-187  
 Kristoff, P.R., and D.P. Nunn. The process specification system for MMST; *T-SEM Aug 95* 262-271  
 Kumar, R.C.K., and J.P. De Gyvez. XFACT: a furnace analysis and characterization tool; *T-SEM Feb 95* 84-87  
 Kuusinen, S.B., *see* Minami, E.R., *T-SEM Aug 95* 370-374

## L

- Lafortune, S., *see* Rashap, B.A., *T-SEM Aug 95* 286-297  
 Lauwers, A., *see* Wang, Q., *T-SEM Nov 95* 449-451  
 Law, M.E. Foreword: Process modeling [special section intro.]; *T-SEM Sept. 1995* 381  
 Lee, S.F., E.D. Boskin, Hao Cheng Liu, E.H. Wen, and C.J. Spanos. RTSPC: a software utility for real-time SPC and tool data analysis; *T-SEM Feb 95* 17-25  
 Lee, S.F., and C.J. Spanos. Prediction of wafer state after plasma processing using real-time tool data; *T-SEM Aug 95* 252-261  
 Lee, T.S., *see* Roedel, R.J., *T-SEM Feb 95* 79-83  
 Lee Yung-Cheng, *see* Jian Tan, *T-SEM Feb 95* 50-61  
 Lee Yung-Cheng, *see* Hong Xie, *T-SEM Aug 95* 219-227  
 Leifer, J., G.Y. Masada, and I.J. Busch-Vishniac. Finite element simulation of a nondestructive shear test for TAB bonds; *T-SEM Aug 95* 352-359  
 Lim, D.H., *see* Morris, S.J., *T-SEM Nov 95* 408-413  
 Liu Hao Cheng, *see* Lee, S.F., *T-SEM Feb 95* 17-25  
 Liu Hua-Yu, *see* Crid Yu, *T-SEM May 95* 150-159

- Loewenstein, L.M., *see* Stefani, J., *T-SEM Feb 95* 2-9  
 Loosen, F., *see* Wang, Q., *T-SEM Nov 95* 449-451  
 Lorenz, J., *see* Bohmayr, W., *T-SEM Nov 95* 402-407  
 Lytle, S.A., *see* Kizilyalli, I.C., *T-SEM Nov 95* 440-448

## M

- Maex, K., *see* Wang, Q., *T-SEM Nov 95* 449-451  
 Mahajan, R.L., *see* Hong Xie, *T-SEM Aug 95* 219-227  
 Maly, W., *see* Khare, J.B., *T-SEM May 95* 195-206  
 Manassian, M., *see* Morris, S.J., *T-SEM Nov 95* 408-413  
 Manikopoulos, C., *see* Belikov, S., *T-SEM Aug 95* 360-362  
 Martin, E.P., Jr., *see* Kizilyalli, I.C., *T-SEM Nov 95* 440-448  
 Martin, W., *see* Collica, R.S., *T-SEM Aug 95* 326-332  
 Martynov, H., *see* Belikov, S., *T-SEM Aug 95* 360-362  
 Masada, G.Y., *see* Leifer, J., *T-SEM Aug 95* 352-359  
 Maung Tinaung, *see* Crid Yu, *T-SEM May 95* 150-159  
 May, G.S., *see* Baker, M.D., *T-SEM Feb 95* 62-71  
 May, G.S., *see* Kenney, J.S., *T-SEM May 95* 207-213  
 Milor, L.S., *see* Chieh-Yuan Chao, *T-SEM Aug 95* 239-251  
 Minami, E.R., S.B. Kuusinen, E. Rosenbaum, P.K. Ko, and Chenming Hu. Circuit-level simulation of TDDDB failure in digital CMOS circuits; *T-SEM Aug 95* 370-374  
 Morris, S.J., S.-H. Yang, D.H. Lim, C. Park, K.M. Klein, M. Manassian, and A.F. Tasch, Jr. An accurate and efficient model for boron implants through thin oxide layers into single-crystal silicon; *T-SEM Nov 95* 408-413  
 Moslehi, B., *see* Weber, C., *T-SEM May 95* 110-120  
 Moyne, J.R., *see* Rashap, B.A., *T-SEM Aug 95* 286-297

## N

- Nakano, K., *see* DeSalvo, G.C., *T-SEM Aug 95* 314-318  
 Nakayama, S., *see* Itsumi, M., *T-SEM Aug 95* 365-370  
 Nanz, G., and L. Camilletti. Modeling of chemical-mechanical polishing: A review; *T-SEM Nov 95* 382-389  
 Neureuther, A.R., *see* Socha, R.J., *T-SEM May 95* 139-149  
 Neureuther, A.R., *see* Wong, A.K., *T-SEM Nov 95* 419-431  
 Nolhier, N., *see* Dilhac, J.-M., *T-SEM Nov 95* 432-439  
 Nunn, D.P., *see* Kristoff, P.R., *T-SEM Aug 95* 262-271

## P

- Park, C., *see* Morris, S.J., *T-SEM Nov 95* 408-413  
 Park, H., O. Smeys, Z.H. Sahul, K.C. Saraswat, R.W. Dutton, and H. Hwang. Quasi-three-dimensional modeling of sub-micron LOCOS structures; *T-SEM Nov 95* 390-401  
 Patel, S.H., *see* Rietman, E.A., *T-SEM Aug 95* 304-308  
 Pease, R.F.W., *see* Jun Ye, *T-SEM Aug 95* 319-325  
 Pelagagge, P.M., *see* Cardarelli, E., *T-SEM Feb 95* 44-49  
 Perkins, R.H., T.J. Riley, and R.S. Gyurcsik. Thermal uniformity and stress minimization during rapid thermal processes; *T-SEM Aug 95* 272-279  
 Pichler, P., *see* Bauer, H., *T-SEM Nov 95* 414-418

## Q

- Quach, T.K., *see* DeSalvo, G.C., *T-SEM Aug 95* 314-318

## R

- Ramhaud, M.M., *see* Kizilyalli, I.C., *T-SEM Nov 95* 440-448  
 Rashap, B.A., M.E. Elta, H. Etemad, J.P. Fournier, J.S. Freudenberg, M.D. Giles, J.W. Grizzle, P.T. Kabamba, P.P. Khargonekar, S. Lafortune, J.R. Moyne, D. Teneketzis, and F.L. Terry, Jr. Control of semiconductor manufacturing equipment: real-time feedback control of a reactive ion etcher; *T-SEM Aug 95* 286-297  
 Reif, R., *see* Zhen-Hong Zhou, *T-SEM Aug 95* 333-339  
 Reif, R., *see* Zhen-Hong Zhou, *T-SEM Aug 95* 340-345  
 Rietman, E.A., and S.H. Patel. A production demonstration of wafer-to-wafer plasma gate etch control by adaptive real-time computation of the over-etch time from in situ process signals; *T-SEM Aug 95* 304-308  
 Riley, P.E., M. Ben-tzur, and R. Kavari. Composite metal etching for submicron integrated circuits; *T-SEM Aug 95* 309-313  
 Riley, T.J., *see* Perkins, R.H., *T-SEM Aug 95* 272-279  
 Robinson, J., *see* Jun Ye, *T-SEM Aug 95* 319-325



- Roedel, R.J., W. West, T.S. Lee, D. Davito, and R. Adams. The fabrication of  $\text{Ga}_{1-x}\text{Al}_x\text{As}$ -GaAs heterojunction bipolar transistors for rapid material analysis; *T-SEM Feb 95* 79-83
- Rosenbaum, E., see Minami, E.R., *T-SEM Aug 95* 370-374
- Rosner, R.J., see Stapper, C.H., *T-SEM May 95* 95-102
- Ryssel, H., see Bohmayr, W., *T-SEM Nov 95* 402-407
- Ryssel, H., see Bauer, H., *T-SEM Nov 95* 414-418

## S

- Sachs, E., A. Hu, and A. Ingolfsson. Run by run process control: combining SPC and feedback control; *T-SEM Feb 95* 26-43
- Sahul, Z.H., see Park, H., *T-SEM Nov 95* 390-401
- Saraswat, K.C., see Park, H., *T-SEM Nov 95* 390-401
- Scheid, E., see Campo, E., *T-SEM Aug 95* 298-303
- Scheid, E., see Henda, R., *T-SEM Aug 95* 362-365
- Schmitt-Landsiedel, D., see Khare, J.B., *T-SEM May 95* 195-206
- Selberherr, S., see Bohmayr, W., *T-SEM Nov 95* 402-407
- Seungil Yu, see Sorrell, F.Y., *T-SEM Aug 95* 280-285
- Singh, R., see Socha, R.J., *T-SEM May 95* 139-149
- Singh, R., see Kizilyalli, I.C., *T-SEM Nov 95* 440-448
- Sitte, R., S. Dimitrijevic, and H.B. Harrison. Relaxation of acceptance limits (RAL): a global approach for parametric yield control of 0.1- $\mu\text{m}$  deep submicron MOSFET devices; *T-SEM Aug 95* 374-377
- Smeys, O., see Park, H., *T-SEM Nov 95* 390-401
- Socha, R.J., A.R. Neureuther, and R. Singh. Models for characterizing phase-shift defects in optical projection printing; *T-SEM May 95* 139-149
- Sorrell, F.Y., M.J. Fordham, and Seungil Yu. A methodology for analysis of RTCVD systems; *T-SEM Aug 95* 280-285
- Spanos, C.J., see Lee, S.F., *T-SEM Feb 95* 17-25
- Spanos, C.J., see Cunningham, S.P., *T-SEM May 95* 103-109
- Spanos, C.J., see Crid Yu, *T-SEM May 95* 150-159
- Spanos, C.J., see Lee, S.F., *T-SEM Aug 95* 252-261
- Stapper, C.H., and R.J. Rosner. Integrated circuit yield management and yield analysis: development and implementation; *T-SEM May 95* 95-102
- Stefani, J., L.M. Loewenstein, and M. Sullivan. On-line diagnostic monitoring of photoresist ashing; *T-SEM Feb 95* 2-9
- Sturm, J.C., see Cullen, C.W., *T-SEM Aug 95* 346-351
- Sullivan, M., see Stefani, J., *T-SEM Feb 95* 2-9
- Sun, W., see Kizilyalli, I.C., *T-SEM Nov 95* 440-448

## T

- Tan Jian, see Jian Tan, *T-SEM Feb 95* 50-61
- Tasch, A.F., Jr., see Morris, S.J., *T-SEM Nov 95* 408-413
- Teneketzi, D., see Rashap, B.A., *T-SEM Aug 95* 286-297
- Terry, F.L., Jr., see Rashap, B.A., *T-SEM Aug 95* 286-297
- Thoma, M.J., see Kizilyalli, I.C., *T-SEM Nov 95* 440-448
- Tinaung Maung, see Crid Yu, *T-SEM May 95* 150-159
- Twiford, M.S., see Kizilyalli, I.C., *T-SEM Nov 95* 440-448

## V

- Venkatraman, P., and B.J. Baliga. Yield loss mechanisms in MOS-gated power devices; *T-SEM Nov 95* 451-453
- Verbeeck, R., see Wang, Q., *T-SEM Nov 95* 449-451
- Via, G.D., see DeSalvo, G.C., *T-SEM Aug 95* 314-318
- Vitkavage, S.C., see Kizilyalli, I.C., *T-SEM Nov 95* 440-448
- Voros, K., see Cunningham, S.P., *T-SEM May 95* 103-109

## W

- Wagner, I.A., and I. Koren. An interactive VLSI CAD tool for yield estimation; *T-SEM May 95* 130-138
- Walker, D.M.H., see Gaitonde, D.D., *T-SEM May 95* 167-177
- Wang, Q., A. Lauwers, B. Deweerdt, R. Verbeeck, F. Loosen, and K. Maex. A manufacturable process to improve thermal stability of 0.25- $\mu\text{m}$  cobalt silicided poly gate; *T-SEM Nov 95* 449-451
- Weber, C., B. Moslehi, and M. Dutta. An integrated framework for yield management and defect/fault reduction; *T-SEM May 95* 110-120
- Wen, E.H., see Lee, S.F., *T-SEM Feb 95* 17-25
- West, W., see Roedel, R.J., *T-SEM Feb 95* 79-83
- Wong, A.K., and A.R. Neureuther. Rigorous three-dimensional time-domain finite-difference electromagnetic simulation for photolithographic applications; *T-SEM Nov 95* 419-431

## X

- Xie Hong, see Jian Tan, *T-SEM Feb 95* 50-61
- Xie Hong, see Hong Xie, *T-SEM Aug 95* 219-227
- Xue Hua, see Huijbregts, E.P., *T-SEM May 95* 188-194

## Y

- Yang, S.-H., see Morris, S.J., *T-SEM Nov 95* 408-413
- Yang Duck-Joo, see Burkett, S.L., *T-SEM Feb 95* 10-16
- Yasuda, H.K., see Burkett, S.L., *T-SEM Feb 95* 10-16
- Ye Jun, see Jun Ye, *T-SEM Aug 95* 319-325
- Yoshino, H., see Itsumi, M., *T-SEM Aug 95* 365-370
- Yu Crid, see Crid Yu, *T-SEM May 95* 150-159
- Yung-Cheng Lee, see Jian Tan, *T-SEM Feb 95* 50-61
- Yung-Cheng Lee, see Hong Xie, *T-SEM Aug 95* 219-227
- Yu Seungil, see Sorrell, F.Y., *T-SEM Aug 95* 280-285

## Z

- Zanchi, C., see Dilhac, J.-M., *T-SEM Nov 95* 432-439
- Zhen-Hong Zhou, and R. Reif. Epi-film thickness measurements using emission Fourier transform infrared spectroscopy. I. Sensor characterization; *T-SEM Aug 95* 333-339
- Zhen-Hong Zhou, and R. Reif. Epi-film thickness measurements using emission Fourier transform infrared spectroscopy. II. Real-time in situ process monitoring and control; *T-SEM Aug 95* 340-345
- Zhou Zhen-Hong, see Zhen-Hong Zhou, *T-SEM Aug 95* 333-339
- Zhou Zhen-Hong, see Zhen-Hong Zhou, *T-SEM Aug 95* 340-345

## SUBJECT INDEX

## A

- Acoustic filters; cf. Surface acoustic wave filters
- Adaptive control  
MOS wafer-to-wafer plasma gate etch control, adaptive real-time computation. Rietman, E.A., +, *T-SEM Aug 95* 304-308
- Adders  
CMOS adder defect spotting, hierarchical mapping. Gaitonde, D.D., +, *T-SEM May 95* 167-177
- Algebra; cf. Vectors
- Aluminum integrated circuit conductors  
CMOS SRAM bit failures, spectrum anal., vector represent. Itsumi, M., +, *T-SEM Aug 95* 365-370
- Ti-W/Al-Cu composite metal etching for submicron IC. Riley, P.E., +, *T-SEM Aug 95* 309-313
- Aluminum materials/devices  
 $\text{Ga}_{1-x}\text{Al}_x\text{As}$ -GaAs HBT, fab. for rapid material anal. Roedel, R.J., +, *T-SEM Feb 95* 79-83
- Applications specific integrated circuits  
high-perform. 3.3/-5-V 0.5- $\mu\text{m}$  CMOS technol. for ASICs. Kizilyalli, I.C., +, *T-SEM Nov 95* 440-448
- Approximation methods; cf. Interpolation; Least squares methods; Polynomial approximation
- Arsenic materials/devices  
modeling dyn. clustering of arsenic. Bauer, H., +, *T-SEM Nov 95* 414-418
- Artificial intelligence; cf. Learning systems
- Automation; cf. Design automation
- Awards  
IEEE Transactions on Semiconductor Manufacturing Best Paper Award given to J.B. Khare, W. Maly, and M.E. Thomas. *T-SEM Aug 95* 218

## B

- Backpropagation  
RIE, time series modeling, neural networks. Baker, M.D., +, *T-SEM Feb 95* 62-71
- SRAM bitmap shape recogn., neural networks. Collica, R.S., +, *T-SEM Aug 95* 326-332
- Binomial distributions  
wafer proc. problems, binomial test tool. Kaempf, U., *T-SEM May 95* 160-166



**Bipolar transistors; cf.** Heterojunction bipolar transistors  
**Bonding; cf.** Integrated circuit bonding; Soldering  
**Boron materials/devices**  
 single-crystal Si, B implants through thin oxide layers, accurate/efficient model. *Morris, S.J.*, +, *T-SEM Nov 95* 408-413  
**Breakdown; cf.** Dielectric breakdown  
**Burn-in programs**  
 digital CMOS ccts., TDDb failure, cct.-level simul. *Minami, E.R.*, +, *T-SEM Aug 95* 370-374

## C

**CAD (computer aided design); cf.** Design automation  
**Charge carrier processes**  
 polysilicon TFTs, elec. props., rapid thermal and low temp. proc. *Campo, E.*, +, *T-SEM Aug 95* 298-303  
**Charge carrier processes; cf.** Surface charging  
**Chemical vapor deposition; cf.** CVD  
**CIM; cf.** Computer integrated manufacturing  
**Circuit modeling; cf.** Integrated circuit modeling  
**Circuit optimization**  
 VLSI design, layout-synthesis, yield enhancement. *Chiluvuri, V.K.R.*, +, *T-SEM May 95* 178-187  
**Circuit reliability; cf.** Integrated circuit reliability  
**Circuits; cf.** Adders; Equivalent circuits  
**Circuit simulation**  
 digital CMOS ccts., TDDb failure, cct.-level simul. *Minami, E.R.*, +, *T-SEM Aug 95* 370-374  
 SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332  
**Circuit testing; cf.** Integrated circuit testing  
**Circuit topology**  
 VLSI design, layout-synthesis, yield enhancement. *Chiluvuri, V.K.R.*, +, *T-SEM May 95* 178-187  
**CMOS digital integrated circuits**  
 TDDb failure, cct.-level simul. *Minami, E.R.*, +, *T-SEM Aug 95* 370-374  
**CMOS digital integrated circuits; cf.** CMOS memory integrated circuits  
**CMOS integrated circuits**  
 adder module, IC defect testing, hierarchical mapping. *Gaitonde, D.D.*, +, *T-SEM May 95* 167-177  
 CoSi<sub>2</sub> salicidation proc., improved thermal stabil. *Wang, Q.*, +, *T-SEM Nov 95* 449-451  
 high-perform. 3.3-/5-V 0.5- $\mu$ m CMOS technol. for ASICs. *Kizilyalli, I.C.*, +, *T-SEM Nov 95* 440-448  
**CMOS integrated circuits; cf.** CMOS digital integrated circuits  
**CMOS memory integrated circuits**  
 SRAM bit failures, spectrum anal., vector representation. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370  
**Computer aided design; cf.** Design automation  
**Computer applications; cf.** Neural network applications  
**Computer integrated manufacturing**  
 MMST, proc. spec. syst., microelectronics CIM. *Kristoff, P.R.*, +, *T-SEM Aug 95* 262-271  
**Contacts; cf.** Ohmic contacts  
**Control systems; cf.** Adaptive control  
**CVD**  
 RTCVD systs. anal., film thickness spatial/temporal distrib. *Sorrell, F.Y.*, +, *T-SEM Aug 95* 280-285  
 thermally based microelectronic mfg. procs., fuzzy logic models. *Hong Xie*, +, *T-SEM Aug 95* 219-227

## D

**Data acquisition**  
 RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71  
**Decision-making; cf.** Pattern classification  
**Design automation**  
 interactive VLSI CAD tool for yield estim. *Wagner, I.A.*, +, *T-SEM May 95* 130-138  
 interbay material handling/storage systs., large wafer fab, simul. tool. *Cardarelli, E.*, +, *T-SEM Feb 95* 44-49  
 VLSI design, layout-synthesis, yield enhancement. *Chiluvuri, V.K.R.*, +, *T-SEM May 95* 178-187  
**Design methodology**  
 yield improvement, short-loop elec. meas. *Crid Yu*, +, *T-SEM May 95* 150-159

**Design methodology; cf.** Design automation

**Dexterous manipulators**

interbay material handling/storage systs., large wafer fab, simul. tool. *Cardarelli, E.*, +, *T-SEM Feb 95* 44-49

**Diagnosis; cf.** Fault diagnosis

**Dielectric breakdown**

digital CMOS ccts., TDDb failure, cct.-level simul. *Minami, E.R.*, +, *T-SEM Aug 95* 370-374

**Diffusion processes**

XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95* 84-87

## E

**Electric breakdown; cf.** Dielectric breakdown

**Electrostatic processes; cf.** Surface charging

**Epitaxial growth**

run by run proc. control combining SPC and feedback control. *Sachs, E.*, +, *T-SEM Feb 95* 26-43

Si, epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 333-339

Si, epitaxial proc. control, emission FT-IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345

**Equivalent circuits**

ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

**Estimation; cf.** Least squares methods; Yield estimation

**Etching**

Ga<sub>1-x</sub>Al<sub>x</sub>As-GaAs HBT, fab. for rapid material anal. *Roedel, R.J.*, +, *T-SEM Feb 95* 79-83

Ti-W/Al-Cu composite metal etching for submicron IC. *Riley, P.E.*, +, *T-SEM Aug 95* 309-313

**Etching; cf.** Sputter etching

## F

**Fabrication; cf.** Semiconductor device fabrication

**Failure analysis**

ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370

digital CMOS ccts., TDDb failure, cct.-level simul. *Minami, E.R.*, +, *T-SEM Aug 95* 370-374

IC routing, reliable mfg. *Huijbregts, E.P.*, +, *T-SEM May 95* 188-194

maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95* 72-78

SRAM, yield-oriented computer-aided defect diagnosis. *Khare, J.B.*, +, *T-SEM May 95* 195-206

**Fault diagnosis**

IC defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95* 121-129

RTSPC, software utility for real-time SPC and tool data anal. *Lee, S.F.*, +, *T-SEM Feb 95* 17-25

**Fault diagnosis; cf.** Memory fault diagnosis

**FDTD methods**

rigorous 3D FDTD EM simul., photolithographic appls. *Wong, A.K.*, +, *T-SEM Nov 95* 419-431

**Feature extraction**

SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332

**Feedback systems**

maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95* 72-78

RIE in semicond. manufacture, real-time feedback control. *Rashap, B.A.*, +, *T-SEM Aug 95* 286-297

run by run proc. control combining SPC and feedback control. *Sachs, E.*, +, *T-SEM Feb 95* 26-43

**Feedforward neural networks**

RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71



**FET integrated circuits; cf.** MOS integrated circuits  
**FET memory integrated circuits; cf.** MOS memory integrated circuits  
**FETs; cf.** MESFETs; Microwave FETs  
**Films; cf.** Semiconductor films  
**Filters; cf.** Surface acoustic wave filters; Transversal filters  
**Fingers; cf.** Dexterous manipulators  
**Finite difference time domain methods; cf.** FDTD methods  
**Finite element methods**  
 TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95 352-359*  
**Force control**  
 maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95 72-78*  
**Fourier spectroscopy**  
 emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95 340-345*  
 epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95 333-339*  
**Functions; cf.** Spline functions  
**Furnaces**  
 XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95 84-87*  
**Fuzzy control**  
 semicond. mfg. proc. modeling and control, fuzzy logic model. *Jian Tan*, +, *T-SEM Feb 95 50-61*  
**Fuzzy logic**  
 thermally based microelectronic mfg. procs., fuzzy logic models. *Hong Xie*, +, *T-SEM Aug 95 219-227*

## G

**Gallium materials/devices**  
 GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95 314-318*  
 Ga<sub>1-x</sub>Al<sub>x</sub>As-GaAs HBT, fab. for rapid material anal. *Roedel, R.J.*, +, *T-SEM Feb 95 79-83*  
**Geometrical optics**  
 RTCVD systs. anal., film thickness spatial/temporal distrib. *Sorrell, F.Y.*, +, *T-SEM Aug 95 280-285*  
**Gradient methods; cf.** Backpropagation  
**Gripping; cf.** Dexterous manipulators

## H

**Hands; cf.** Dexterous manipulators  
**Heat treatment; cf.** Rapid thermal processing  
**Heterojunction bipolar transistors**  
 Ga<sub>1-x</sub>Al<sub>x</sub>As-GaAs HBT, fab. for rapid material anal. *Roedel, R.J.*, +, *T-SEM Feb 95 79-83*

## I

**IEEE Transactions on Semiconductor Manufacturing; cf.** Awards  
**IGFETs; cf.** MOSFETs  
**Industrial control; cf.** Process control  
**Infrared detectors**  
 epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95 333-339*  
**Infrared spectroscopy**  
 emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95 340-345*  
 epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95 333-339*  
 Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95 346-351*  
**Integrated circuit bonding**  
 TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95 352-359*  
**Integrated circuit design**  
 CMOS adder defect spotting, hierarchical mapping. *Gaitonde, D.D.*, +, *T-SEM May 95 167-177*  
**Integrated circuit design; cf.** Layout of integrated circuits  
**Integrated circuit economics**  
 routing, reliable mfg. *Huijbregts, E.P.*, +, *T-SEM May 95 188-194*  
**Integrated circuit fabrication; cf.** Integrated circuit bonding; Integrated circuit manufacture; Lithography; Resists  
**Integrated circuit interconnections**  
 defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95 121-129*

TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95 352-359*

**Integrated circuit interconnections; cf.** Aluminum integrated circuit conductors

#### Integrated circuit manufacture

CoSi<sub>2</sub> salicidation proc., improved thermal stabil. *Wang, Q.*, +, *T-SEM Nov 95 449-451*  
 defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95 121-129*  
 interbay material handling/storage systs., large wafer fab, simul. tool. *Cardarelli, E.*, +, *T-SEM Feb 95 44-49*  
 maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95 72-78*  
 MMST, proc. spec. syst., microelectronics CIM. *Kristoff, P.R.*, +, *T-SEM Aug 95 262-271*  
 MOS wafer-to-wafer plasma gate etch control, adaptive real-time computation. *Rietman, E.A.*, +, *T-SEM Aug 95 304-308*  
 run by run proc. control combining SPC and feedback control. *Sachs, E.*, +, *T-SEM Feb 95 26-43*  
 Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95 346-351*  
 VLSI proc. improvement, proc. noise effects, simul. *Bohn, R.E.*, *T-SEM Aug 95 228-238*  
 wafer proc. problems, binomial test tool. *Kaempf, U.*, *T-SEM May 95 160-166*  
 XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95 84-87*

#### Integrated circuit measurements

VLSI mfg., mask errors on variety of pattern generators. *Jun Ye*, +, *T-SEM Aug 95 319-325*  
 yield improvement, short-loop elec. meas. *Crid Yu*, +, *T-SEM May 95 150-159*

#### Integrated circuit mechanical factors

TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95 352-359*

**Integrated circuit metallization; cf.** Aluminum integrated circuit conductors; Integrated circuit interconnections

#### Integrated circuit modeling

ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95 207-213*  
 defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95 121-129*  
 TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95 352-359*

#### Integrated circuit reliability

CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95 365-370*  
 defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95 121-129*  
 digital CMOS ccts., TDDB failure, cct.-level simul. *Minami, E.R.*, +, *T-SEM Aug 95 370-374*  
 routing, reliable mfg. *Huijbregts, E.P.*, +, *T-SEM May 95 188-194*  
 TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95 352-359*

#### Integrated circuit testing

CMOS adder defect spotting, hierarchical mapping. *Gaitonde, D.D.*, +, *T-SEM May 95 167-177*  
 wafer proc. problems, binomial test tool. *Kaempf, U.*, *T-SEM May 95 160-166*

#### Integrated circuit thermal factors

RTP furnace, thermal behavior model. *Henda, R.*, +, *T-SEM Aug 95 362-365*  
 wafer, heat transfer in RTP, wavelength-depend. emissivity model. *Belikov, S.*, +, *T-SEM Aug 95 360-362*

#### Interactive systems

VLSI CAD tool for yield estim. *Wagner, I.A.*, +, *T-SEM May 95 130-138*

**Interconnections; cf.** Integrated circuit interconnections

#### Interpolation

XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95 84-87*



**Interpolation;** cf. Spline functions  
**Ion implantation;** cf. Semiconductor device ion implantation

## K

**Kohonen networks;** cf. Self-organizing feature maps

## L

**Large-scale integration;** cf. Ultra-large-scale integration; Very-large-scale integration

**Layout of integrated circuits**

IC routing, reliable mfg. *Huijbregts, E.P.*, +, *T-SEM May 95* 188-194  
 interactive VLSI CAD tool for yield estim. *Wagner, I.A.*, +, *T-SEM May 95* 130-138  
 routing, reliable mfg. *Huijbregts, E.P.*, +, *T-SEM May 95* 188-194  
 VLSI design, layout-synthesis, yield enhancement. *Chiluvuri, V.K.R.*, +, *T-SEM May 95* 178-187

**Learning systems**

SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332

**Learning systems;** cf. Backpropagation**Least mean square methods;** cf. Backpropagation**Least squares methods**

wafer state prediction, plasma etch proc., real-time tool data. *Lee, S.F.*, +, *T-SEM Aug 95* 252-261

**Levitation;** cf. Magnetic levitation**Lithography**

GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95* 314-318  
 VLSI mfg., mask errors on variety of pattern generators. *Jun Ye*, +, *T-SEM Aug 95* 319-325  
 yield improvement, short-loop elec. meas. *Crid Yu*, +, *T-SEM May 95* 150-159

**Lithography;** cf. Photolithography**Logic;** cf. Fuzzy logic

## M

**Magnetic levitation**

contact anal. probe tool, automated IC anal. probing stations. *Chen, S.-J.S.*, +, *T-SEM Feb 95* 72-78

**Management;** cf. Production management**Manipulators;** cf. Dexterous manipulators**Manufacturing automation;** cf. Computer integrated manufacturing**Manufacturing automation software**

XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95* 84-87

**Manufacturing scheduling**

MMST, proc. spec. syst., microelectronics CIM. *Kristoff, P.R.*, +, *T-SEM Aug 95* 262-271

**Manufacturing testing**

maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95* 72-78

**Masks**

opt. projection printing, phase-shift defects, model. *Socha, R.J.*, +, *T-SEM May 95* 139-149  
 semicond. wafer cleaning procedure, effects on surface charging of substs. *Burkett, S.L.*, +, *T-SEM Feb 95* 10-16  
 VLSI mfg., mask errors on variety of pattern generators. *Jun Ye*, +, *T-SEM Aug 95* 319-325

**Materials handling**

interbay material handling/storage systs., large wafer fab, simul. tool. *Cardarelli, E.*, +, *T-SEM Feb 95* 44-49

**Materials processing;** cf. Etching; Plasma materials-processing applications**Materials testing;** cf. Nondestructive testing**Measurement;** cf. Integrated circuit measurements**Mechanical factors;** cf. Integrated circuit mechanical factors**Mechanical variables control;** cf. Force control; Position control; Pressure control; Thickness control**Mechanical variables measurement;** cf. Thickness measurement**Memories;** cf. SRAM chips**Memory fault diagnosis**

CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370  
 SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332  
 SRAM, yield-oriented computer-aided defect diagnosis. *Khare, J.B.*, +, *T-SEM May 95* 195-206

**MESFETs**

GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95* 314-318

**Metallization;** cf. Semiconductor device metallization**Metal materials/devices;** cf. Aluminum materials/devices; Boron materials/devices; Gallium materials/devices**Metal-semiconductor devices;** cf. MESFETs**Microwave FETs**

GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95* 314-318

**MISFETs;** cf. MOSFETs**Modeling**

advanced yield modeling (special issue). *T-SEM May 95* 93-213

**Modeling;** cf. Semiconductor process modeling; Simulation**Monitoring;** cf. Process monitoring**Monte Carlo methods**

ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

ion implant., Monte Carlo simul., trajectory split method. *Bohmayr, W.*, +, *T-SEM Nov 95* 402-407

**MOS devices;** cf. MOSFETs**MOS digital integrated circuits;** cf. CMOS digital integrated circuits; MOS memory integrated circuits**MOSFETs**

0.1- $\mu$ m, parametric yield control, relax. of acceptance limits. *Sitte, R.*, +, *T-SEM Aug 95* 374-377

**MOSFETs;** cf. Power MOSFETs**MOS integrated circuits**

wafer-to-wafer plasma gate etch control, adaptive real-time computation. *Rietman, E.A.*, +, *T-SEM Aug 95* 304-308

**MOS integrated circuits;** cf. CMOS integrated circuits**MOS memory integrated circuits**

interbay material handling/storage systs., large wafer fab, simul. tool. *Cardarelli, E.*, +, *T-SEM Feb 95* 44-49

**MOS memory integrated circuits;** cf. CMOS memory integrated circuits**Multidimensional systems;** cf. Multivariable systems**Multiinput-multioutput systems;** cf. Multivariable systems**Multilayer perceptrons**

SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332

**Multivariable systems**

RIE in semicond. manufacture, real-time feedback control. *Rashap, B.A.*, +, *T-SEM Aug 95* 286-297

## N

**Neural network applications**

RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71

SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332

wafer state prediction, plasma etch proc., real-time tool data. *Lee, S.F.*, +, *T-SEM Aug 95* 252-261

**Neural networks;** cf. Feedforward neural networks; Multilayer perceptrons; Self-organizing feature maps**Nondestructive testing**

TAB bonds, nondestructive shear test, FEM simul. *Leifer, J.*, +, *T-SEM Aug 95* 352-359

**Nonlinear systems**

MOS wafer-to-wafer plasma gate etch control, adaptive real-time computation. *Rietman, E.A.*, +, *T-SEM Aug 95* 304-308

**Numerical analysis;** cf. Finite element methods; Monte Carlo methods

## O

**Ohmic contacts**

GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95* 314-318

**Optics;** cf. Geometrical optics**Optimization methods;** cf. Circuit optimization; Least squares methods

## P

**Packaging;** cf. Semiconductor device packaging**Pattern classification**

SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332



**Perceptrons; cf. Multilayer perceptrons****Photolithography**

- projection printing, phase-shift defects, model. *Socha, R.J.*, +, *T-SEM May 95* 139-149
- rigorous 3D FDTD EM simul., photolithographic appls. *Wong, A.K.*, +, *T-SEM Nov 95* 419-431
- semicond. wafer cleaning procedure, effects on surface charging of substrs. *Burkett, S.L.*, +, *T-SEM Feb 95* 10-16

**Plasma materials-processing applications**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345

**Poisson distributions**

- ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

**Polynomial approximation**

- wafer, heat transfer in RTP, wavelength-depend. emissivity model. *Belikov, S.*, +, *T-SEM Aug 95* 360-362

**Position control**

- maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95* 72-78

**Power MOSFETs**

- MOS-gated power device yield loss mechanisms. *Venkatraman, P.*, +, *T-SEM Nov 95* 451-453

**Pressure control**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345

**Printing**

- opt. projection printing, phase-shift defects, model. *Socha, R.J.*, +, *T-SEM May 95* 139-149

**Probability**

- CMOS adder defect spotting, hierarchical mapping. *Gaitonde, D.D.*, +, *T-SEM May 95* 167-177

**Probability; cf. Binomial distributions; Monte Carlo methods; Poisson distributions****Process control**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345
- MOS wafer-to-wafer plasma gate etch control, adaptive real-time computation. *Rietman, E.A.*, +, *T-SEM Aug 95* 304-308
- RIE in semicond. manufacture, real-time feedback control. *Rashap, B.A.*, +, *T-SEM Aug 95* 286-297
- RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71
- run by run proc. control combining SPC and feedback control. *Sachs, E.*, +, *T-SEM Feb 95* 26-43
- semicond. mfg. proc. modeling and control, fuzzy logic model. *Jian Tan*, +, *T-SEM Feb 95* 50-61
- semicond. yield improvement. *Cunningham, S.P.*, +, *T-SEM May 95* 103-109

**Process monitoring**

- CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370
- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345
- epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 333-339
- IC defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95* 121-129
- interbay material handling/storage systs., large wafer fab, simul. tool. *Cardarelli, E.*, +, *T-SEM Feb 95* 44-49
- maglev contact anal. probe tool for automated IC manufacture. *Chen, S.-J.S.*, +, *T-SEM Feb 95* 72-78
- RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71
- RTSPC, software utility for real-time SPC and tool data anal. *Lee, S.F.*, +, *T-SEM Feb 95* 17-25
- semicond. mfg., photoresist ashing, on-line diagnostic monitoring. *Stefani, J.*, +, *T-SEM Feb 95* 2-9
- Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95* 346-351

**Production management**

- IC yield mgt. and yield anal. *Stapper, C.H.*, +, *T-SEM May 95* 95-102
- MMST, proc. spec. syst., microelectronics CIM. *Kristoff, P.R.*, +, *T-SEM Aug 95* 262-271

**Protection/safety**

- RTSPC, software utility for real-time SPC and tool data anal. *Lee, S.F.*, +, *T-SEM Feb 95* 17-25

**Q****Quality assurance**

- IC yield mgt. and defect/fault reduction, integrated framework. *Weber, C.*, +, *T-SEM May 95* 110-120
- MOSFET, 0.1- $\mu$ m, parametric yield control, relax. of acceptance limits. *Sitte, R.*, +, *T-SEM Aug 95* 374-377

**Quality control**

- CMOS adder defect spotting, hierarchical mapping. *Gaitonde, D.D.*, +, *T-SEM May 95* 167-177
- IC defect data anal., quality and reliab. impact. *Bruls, E.*, *T-SEM May 95* 121-129
- MMST, proc. spec. syst., microelectronics CIM. *Kristoff, P.R.*, +, *T-SEM Aug 95* 262-271

**R****Radiation detectors; cf. Infrared detectors****Random access memories; cf. SRAM chips****Rapid thermal processing**

- polysilicon TFTs, elec. props., rapid thermal and low temp. proc. *Campo, E.*, +, *T-SEM Aug 95* 298-303
- RTCVD systs. anal., film thickness spatial/temporal distrib. *Sorrell, F.Y.*, +, *T-SEM Aug 95* 280-285
- Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95* 346-351
- thermal behavior of RTP furnace, model. *Henda, R.*, +, *T-SEM Aug 95* 362-365
- thermal modeling of wafer in rapid thermal processor. *Dilhac, J.-M.*, +, *T-SEM Nov 95* 432-439
- uniformity and stress minimization, rapid thermal procs. *Perkins, R.H.*, +, *T-SEM Aug 95* 272-279
- wafer, heat transfer in RTP, wavelength-depend. emissivity model. *Belikov, S.*, +, *T-SEM Aug 95* 360-362

**Ray optics; cf. Geometrical optics****Real time systems**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345
- MOS wafer-to-wafer plasma gate etch control, adaptive real-time computation. *Rietman, E.A.*, +, *T-SEM Aug 95* 304-308
- RIE in semicond. manufacture, real-time feedback control. *Rashap, B.A.*, +, *T-SEM Aug 95* 286-297
- RTSPC, software utility for real-time SPC and tool data anal. *Lee, S.F.*, +, *T-SEM Feb 95* 17-25

**Redundancy**

- ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

**Reliability; cf. Burn-in programs; Failure analysis; Quality control****Resists**

- semicond. mfg., photoresist ashing, on-line diagnostic monitoring. *Stefani, J.*, +, *T-SEM Feb 95* 2-9
- Ti-W/Al-Cu composite metal etching for submicron IC. *Riley, P.E.*, +, *T-SEM Aug 95* 309-313

**Resource management**

- IC yield mgt. and yield anal. *Stapper, C.H.*, +, *T-SEM May 95* 95-102

**Rough surfaces**

- Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95* 346-351

**S****Safety; cf. Protection/safety****Scheduling; cf. Manufacturing scheduling****Schottky FETs; cf. MESFETs****Self-organizing feature maps**

- SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332

**Semiconductor device bonding; cf. Integrated circuit bonding****Semiconductor device doping; cf. Semiconductor device ion implantation****Semiconductor device economics; cf. Integrated circuit economics****Semiconductor device fabrication**

- cleaning procedures, surface charging of substrs. *Burkett, S.L.*, +, *T-SEM Feb 95* 10-16
- GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95* 314-318

**Semiconductor device fabrication; cf. Lithography; Semiconductor device manufacture; Semiconductor device metallization; Semiconductor device packaging****Semiconductor device ion implantation**

- modeling dyn. clustering of arsenic. *Bauer, H.*, +, *T-SEM Nov 95* 414-418



- Monte Carlo simul., trajectory split method. *Bohmayr, W.*, +, *T-SEM Nov 95* 402-407
- single-crystal Si, B implants through thin oxide layers, accurate/efficient model. *Morris, S.J.*, +, *T-SEM Nov 95* 408-413
- Semiconductor device manufacture**
- fuzzy logic model, semicond. proc. control. *Jian Tan*, +, *T-SEM Feb 95* 50-61
- high-perform. 3.3-/5-V 0.5- $\mu$ m CMOS technol. for ASICs. *Kizilyalli, I.C.*, +, *T-SEM Nov 95* 440-448
- MOSFET, 0.1- $\mu$ m, parametric yield control, relax. of acceptance limits. *Sitte, R.*, +, *T-SEM Aug 95* 374-377
- MOS-gated power device yield loss mechanisms. *Venkatraman, P.*, +, *T-SEM Nov 95* 451-453
- photoresist ashing, on-line diagnostic monitoring. *Stefani, J.*, +, *T-SEM Feb 95* 2-9
- RIE in semicond. manufacture, real-time feedback control. *Rashap, B.A.*, +, *T-SEM Aug 95* 286-297
- RTSPC, software utility for real-time SPC and tool data anal. *Lee, S.F.*, +, *T-SEM Feb 95* 17-25
- thermally based microelectronic mfg. procs., fuzzy logic models. *Hong Xie*, +, *T-SEM Aug 95* 219-227
- uniformity and stress minimization, rapid thermal procs. *Perkins, R.H.*, +, *T-SEM Aug 95* 272-279
- yield improvement. *Cunningham, S.P.*, +, *T-SEM May 95* 103-109
- Semiconductor device manufacture; cf.** Semiconductor device fabrication
- Semiconductor device measurements; cf.** Integrated circuit measurements
- Semiconductor device mechanical factors; cf.** Integrated circuit mechanical factors
- Semiconductor device metallization**
- GaAs SLIMFET, ohmic/Schottky contact form. *DeSalvo, G.C.*, +, *T-SEM Aug 95* 314-318
- Ga<sub>1-x</sub>Al<sub>x</sub>As-GaAs HBT, fab. for rapid material anal. *Roedel, R.J.*, +, *T-SEM Feb 95* 79-83
- Semiconductor device modeling; cf.** Integrated circuit modeling
- Semiconductor device packaging**
- fuzzy logic model, semicond. proc. control. *Jian Tan*, +, *T-SEM Feb 95* 50-61
- Semiconductor device reliability; cf.** Integrated circuit reliability
- Semiconductor device testing; cf.** Integrated circuit testing
- Semiconductor device thermal factors**
- thermal modeling of wafer in rapid thermal processor. *Dilhac, J.-M.*, +, *T-SEM Nov 95* 432-439
- Semiconductor device thermal factors; cf.** Integrated circuit thermal factors
- Semiconductor films**
- Si, epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 333-339
- Si, epitaxial proc. control, emission FT-IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345
- Semiconductor growth**
- run by run proc. control combining SPC and feedback control. *Sachs, E.*, +, *T-SEM Feb 95* 26-43
- Si, epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 333-339
- Si, epitaxial proc. control, emission FT-IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345
- Semiconductor materials; cf.** Semiconductor films
- Semiconductor process modeling**
- chem.-mech. polishing modeling, review. *Nanz, G.*, +, *T-SEM Nov 95* 382-389
- ion implant., Monte Carlo simul., trajectory split method. *Bohmayr, W.*, +, *T-SEM Nov 95* 402-407
- LOCOS structs., submicron, quasi-3D modeling. *Park, H.*, +, *T-SEM Nov 95* 390-401
- modeling dyn. clustering of arsenic. *Bauer, H.*, +, *T-SEM Nov 95* 414-418
- opt. projection printing, phase-shift defects, model. *Socha, R.J.*, +, *T-SEM May 95* 139-149
- RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71
- rigorous 3D FDTD EM simul., photolithographic appls. *Wong, A.K.*, +, *T-SEM Nov 95* 419-431
- RTCVD systs. anal., film thickness spatial/temporal distrib. *Sorrell, F.Y.*, +, *T-SEM Aug 95* 280-285
- RTP furnace, thermal behavior model. *Henda, R.*, +, *T-SEM Aug 95* 362-365
- single-crystal Si, B implants through thin oxide layers, accurate/efficient model. *Morris, S.J.*, +, *T-SEM Nov 95* 408-413
- SRAM, yield-oriented computer-aided defect diagnosis. *Khare, J.B.*, +, *T-SEM May 95* 195-206
- TCAD: process modeling (special section). *T-SEM Sept. 1995* 381-431
- thermally based microelectronic mfg. procs., fuzzy logic models. *Hong Xie*, +, *T-SEM Aug 95* 219-227
- thermal modeling of wafer in rapid thermal processor. *Dilhac, J.-M.*, +, *T-SEM Nov 95* 432-439
- uniformity and stress minimization, rapid thermal procs. *Perkins, R.H.*, +, *T-SEM Aug 95* 272-279
- VLSI proc. improvement, proc. noise effects, simul. *Bohn, R.E.*, *T-SEM Aug 95* 228-238
- VLSI yield perform. modeling, additive regression splines. *Chieh-Yuan Chao*, +, *T-SEM Aug 95* 239-251
- wafer, heat transfer in RTP, wavelength-depend. emissivity model. *Belikov, S.*, +, *T-SEM Aug 95* 360-362
- wafer state prediction, plasma etch proc., real-time tool data. *Lee, S.F.*, +, *T-SEM Aug 95* 252-261
- XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95* 84-87
- Sensitivity**
- interactive VLSI CAD tool for yield estim. *Wagner, I.A.*, +, *T-SEM May 95* 130-138
- MOSFET, 0.1- $\mu$ m, parametric yield control, relax. of acceptance limits. *Sitte, R.*, +, *T-SEM Aug 95* 374-377
- Signal analysis; cf.** Spectral analysis
- Silicon materials/devices**
- epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 333-339
- epitaxial proc. control, emission FT-IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345
- polysilicon TFTs, elec. props., rapid thermal and low temp. proc. *Campo, E.*, +, *T-SEM Aug 95* 298-303
- run by run proc. control combining SPC and feedback control. *Sachs, E.*, +, *T-SEM Feb 95* 26-43
- single-crystal Si, B implants through thin oxide layers, accurate/efficient model. *Morris, S.J.*, +, *T-SEM Nov 95* 408-413
- Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95* 346-351
- Simulation**
- ion implant., Monte Carlo simul., trajectory split method. *Bohmayr, W.*, +, *T-SEM Nov 95* 402-407
- LOCOS structs., submicron, quasi-3D modeling. *Park, H.*, +, *T-SEM Nov 95* 390-401
- XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95* 84-87
- Simulation; cf.** Circuit simulation
- Simulation software**
- rigorous 3D FDTD EM simul., photolithographic appls. *Wong, A.K.*, +, *T-SEM Nov 95* 419-431
- Size control; cf.** Thickness control
- Size measurement; cf.** Thickness measurement
- Software; cf.** Manufacturing automation software; Simulation software
- Soldering**
- thermally based microelectronic mfg. procs., fuzzy logic models. *Hong Xie*, +, *T-SEM Aug 95* 219-227
- Special issues/sections**
- advanced yield modeling (special issue). *T-SEM May 95* 93-213
- TCAD: process modeling (special section). *T-SEM Sept. 1995* 381-431
- Spectral analysis**
- CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370
- Spectroscopy; cf.** Fourier spectroscopy; Infrared spectroscopy
- Spline functions**
- VLSI yield perform. modeling, additive regression splines. *Chieh-Yuan Chao*, +, *T-SEM Aug 95* 239-251
- Sputter etching**
- MOS wafer-to-wafer plasma gate etch control, adaptive real-time computation. *Rietman, E.A.*, +, *T-SEM Aug 95* 304-308
- RIE in semicond. manufacture, real-time feedback control. *Rashap, B.A.*, +, *T-SEM Aug 95* 286-297
- RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71
- RTSPC, software utility for real-time SPC and tool data anal. *Lee, S.F.*, +, *T-SEM Feb 95* 17-25
- semicond. mfg., photoresist ashing, on-line diagnostic monitoring. *Stefani, J.*, +, *T-SEM Feb 95* 2-9
- wafer state prediction, plasma etch proc., real-time tool data. *Lee, S.F.*, +, *T-SEM Aug 95* 252-261
- SRAM chips**
- bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332
- CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370
- yield-oriented computer-aided defect diagnosis. *Khare, J.B.*, +, *T-SEM May 95* 195-206



**Statistics**

- VLSI yield perform. modeling, additive regression splines. *Chieh-Yuan Chao*, +, *T-SEM Aug 95* 239-251  
 wafer proc. problems, binomial test tool. *Kaempfer, U.*, *T-SEM May 95* 160-166  
 wafer state prediction, plasma etch proc., real-time tool data. *Lee, S.F.*, +, *T-SEM Aug 95* 252-261

**Stochastic processes; cf. Time series****Surface acoustic wave filters**

- ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

**Surface charging**

- semicond. wafer cleaning procedure, effects on surface charging of substs. *Burkett, S.L.*, +, *T-SEM Feb 95* 10-16

**Surfaces; cf. Rough surfaces****T****Temperature control**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345

**Temperature measurement**

- Si wafers, metal-coated, temp. meas., double-pass IR transm. *Cullen, C.W.*, +, *T-SEM Aug 95* 346-351

**Testing; cf. Manufacturing testing; Nondestructive testing****Thermal factors**

- XFACT, diffusion furnace anal. and charactn. tool. *Kumar, R.C.K.*, +, *T-SEM Feb 95* 84-87

**Thermal factors; cf. Integrated circuit thermal factors; Semiconductor device thermal factors****Thermal variables control; cf. Temperature control****Thermal variables measurement; cf. Temperature measurement****Thickness control**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345

**Thickness measurement**

- emission FT-IR spectrosc., real-time epitaxial proc. control. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 340-345  
 epi-film thickness meas., emission FTIR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Aug 95* 333-339

**Thin film transistors**

- polysilicon TFTs, elec. props., rapid thermal and low temp. proc. *Campo, E.*, +, *T-SEM Aug 95* 298-303

**Time domain analysis; cf. FDTD methods****Time series**

- RIE, time series modeling, neural networks. *Baker, M.D.*, +, *T-SEM Feb 95* 62-71

**Titanium materials/devices**

- Ti-W/Al-Cu composite metal etching for submicron IC. *Riley, P.E.*, +, *T-SEM Aug 95* 309-313

**Tolerance analysis/assignment**

- MOSFET, 0.1- $\mu$ m, parametric yield control, relax. of acceptance limits. *Sitte, R.*, +, *T-SEM Aug 95* 374-377

**Topology; cf. Circuit topology****Transistors; cf. Thin film transistors****Transition metal materials/devices; cf. Titanium materials/devices; Tungsten materials/devices****Transversal filters**

- ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213

**Tungsten materials/devices**

- Ti-W/Al-Cu composite metal etching for submicron IC. *Riley, P.E.*, +, *T-SEM Aug 95* 309-313

**U****Ultra-large-scale integration**

- yield mgt. and defect/fault reduction, integrated framework. *Weber, C.*, +, *T-SEM May 95* 110-120

**V****Vapor deposition; cf. CVD****Vectors**

- CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370

**Very-large-scale integration**

- CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370  
 design, layout-synthesis, yield enhancement. *Chiluvuri, V.K.R.*, +, *T-SEM May 95* 178-187  
 interactive VLSI CAD tool for yield estim. *Wagner, I.A.*, +, *T-SEM May 95* 130-138  
 mask dimens. errors, pattern generators, VLSI mfg. *Jun Ye*, +, *T-SEM Aug 95* 319-325  
 proc. improvement, proc. noise effects. *Bohn, R.E.*, *T-SEM Aug 95* 228-238  
 Ti-W/Al-Cu composite metal etching for submicron IC. *Riley, P.E.*, +, *T-SEM Aug 95* 309-313  
 yield mgt. and defect/fault reduction, integrated framework. *Weber, C.*, +, *T-SEM May 95* 110-120  
 yield perform. modeling, additive regression splines. *Chieh-Yuan Chao*, +, *T-SEM Aug 95* 239-251

**Very-large-scale integration; cf. Wafer-scale integration****Voltage breakdown; cf. Dielectric breakdown****W****Wafer-scale integration**

- wafer proc. problems, binomial test tool. *Kaempfer, U.*, *T-SEM May 95* 160-166

**Y****Yield estimation**

- ACT transversal filters, yield modeling. *Kenney, J.S.*, +, *T-SEM May 95* 207-213  
 advanced yield modeling (special issue). *T-SEM May 95* 93-213  
 CMOS adder defect spotting, hierarchical mapping. *Gaitonde, D.D.*, +, *T-SEM May 95* 167-177  
 CMOS SRAM bit failures, spectrum anal., vector represent. *Itsumi, M.*, +, *T-SEM Aug 95* 365-370  
 integrated framework for yield mgt. and defect/fault reduction. *Weber, C.*, +, *T-SEM May 95* 110-120  
 interactive VLSI CAD tool for yield estim. *Wagner, I.A.*, +, *T-SEM May 95* 130-138  
 mgt. and anal. *Stapper, C.H.*, +, *T-SEM May 95* 95-102  
 semicond. yield improvement. *Cunningham, S.P.*, +, *T-SEM May 95* 103-109  
 short-loop elec. meas. *Crid Yu*, +, *T-SEM May 95* 150-159  
 SRAM bitmap shape recogn., neural networks. *Collica, R.S.*, +, *T-SEM Aug 95* 326-332  
 SRAM, yield-oriented computer-aided defect diagnosis. *Khare, J.B.*, +, *T-SEM May 95* 195-206  
 VLSI design, layout-synthesis, yield enhancement. *Chiluvuri, V.K.R.*, +, *T-SEM May 95* 178-187  
 VLSI mfg., mask errors on variety of pattern generators. *Jun Ye*, +, *T-SEM Aug 95* 319-325  
 wafer proc. problems, binomial test tool. *Kaempfer, U.*, *T-SEM May 95* 160-166

**Yield optimization**

- advanced yield modeling (special issue). *T-SEM May 95* 93-213  
 MOSFET, 0.1- $\mu$ m, parametric yield control, relax. of acceptance limits. *Sitte, R.*, +, *T-SEM Aug 95* 374-377  
 MOS-gated power device yield loss mechanisms. *Venkatraman, P.*, +, *T-SEM Nov 95* 451-453  
 VLSI proc. improvement, proc. noise effects, simul. *Bohn, R.E.*, *T-SEM Aug 95* 228-238  
 VLSI yield perform. modeling, additive regression splines. *Chieh-Yuan Chao*, +, *T-SEM Aug 95* 239-251





# INTERNATIONAL SEMICONDUCTOR CONFERENCE

19th Edition

Sinaia, Romania, 9 - 12 October, 1996



## CALL FOR PAPERS - First Announcement



The 19th edition of the **International Semiconductor Conference (CAS)**, is organized by the **Research Institute for Electronic Components (ICCE)**, co-sponsored by IEEE Electron Devices Society, IEEE - Romania Section, the Ministry of Research and Technology, the **SOROS** Foundation and under the aegis of the Romanian Academy and IEEE Electron Devices Chapter.

The aim of the conference is to bring together scientists and engineers actively engaged in the field of solid state devices and technologies. CAS intends to provide a forum for presentation and discussion of the main achievements in physics, design, technology and application of semiconductor devices and materials.

### INTERNATIONAL ADVISORY COMMITTEE

**S.Cristoloveanu** - CNRS, Grenoble, France

**D.Dascalu** - Inst. for Microtechnology,  
Romania

**R.B.Fair** - Center for Microelectronics, NC, USA

**U.Goesele** - Duke University, NC, USA

**R.Grigorovici** - Romanian Academy, Romania

**H.G.Grimmeiss** - Lund University, Sweden

**S.M.Hu** - IBM, NY, USA

**H.Luth** - Inst.of.Thin Films and Ion  
Technology, Julich, Germany

**A.Mircea** - CNET, Bagneux, France

**I.Mojzes** - Technical University, Hungary

**Y.Okuto** - NEC. Corp., Japan

**R.van Overstraeten** - IMEC, Belgium

**M.Profirescu** - Politehnica University, Romania

**S.Radautsan** - Academy of Sciences, Moldova

**S.Selberherr** - Technical University Vienna,  
Austria

**N.Stojadinovic** - Nis University, Yugoslavia

**K.Sumino** - Tohoku University, Japan

**S.M.Sze** - National Chiao Tung Univ.,  
Taiwan, ROC

**F.J.Tegude** - Duisburg University, Germany

**A.Tugulea** - "Politehnica" University, Romania

### TECHNICAL PROGRAM

Papers are solicited in the following areas:

Semiconductor device physics and modeling; Processing technologies; Monolithic and hybrid integrated circuits; Microwave devices; Optoelectronic devices; Semiconductor sensors; Power semiconductor devices; Reliability and defect engineering; Testing; Applications.

### ABSTRACT TO BE SUBMITTED

The CAS '96 program will consist in invited papers and regular papers (structured in oral or poster sessions).

Regular papers will be selected on the basis of a submitted extended abstract (4 pages A4, including a 50 words summary, figures and references), original + 4 copies, written in English.

The extended abstracts will be published in the CAS '96 Proceedings. The papers are printed exactly as they are sent, by direct reproduction (photo-offset), without reducing dimensions.

Due to the publishing requests, the authors should edit and print the papers **on computer, in very good contrast conditions**, ("Roman" type font - min. 10pt. is recommended) on A4 size bond paper.

**DEADLINES** - **15th April 1996**: Submission of the extended abstract.

- **10th July 1996**: Notification of the final acceptance of regular papers.

### GENERAL INFORMATION

**OFFICIAL LANGUAGE**: English.

**LOCATION**: Sinaia is a beautiful mountain resort located at about 120 km NW from Bucharest.

**CONFERENCE FEE** : 150 USD (IEEE non-member), 120 USD (IEEE member), 50 USD (student).

**REGISTRATION FORM**:

The Registration Form will be sent to the authors together with the final notification of the papers' acceptance.

The papers will be sent to:

**Doina VANCU**, Organizing Committee Chairwoman  
ICCE, Str. Erou Iancu Nicolae 32B, 72996 - **Bucharest, ROMANIA**  
Fax : +401 312 75 19 / Phone : +401 633 30 40